2N7000
2N7002

N-CHANNEL 60V - 1.8Ω - 0.35A SOT23-3L - TO-92
STripFET™II MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_d
2N7000	60 V	< 5 Ω (@ 10V)	0.35 A
2N7002	60 V	< 5 Ω (@ 10V)	0.20 A

- TYPICAL $R_{DS}(on)$ = 1.8Ω @10V
- LOW Q_g
- LOW THRESHOLD DRIVE

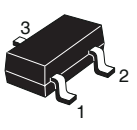
DESCRIPTION

This MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

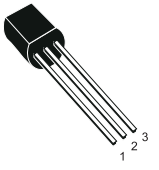
APPLICATIONS

- HIGH SWITCHING APPLICATIONS

Figure 1: Package

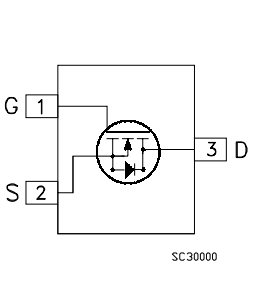


SOT23-3L

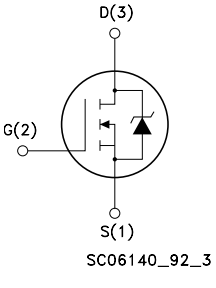


TO-92

Figure 2: Internal Schematic Diagram



SOT23-3L



TO-92

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
2N7000	2N7000G	TO-92	BULK
2N7002	ST2N	SOT23-3L	TAPE & REEL

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate- source Voltage	± 18		V
I_D	Drain Current (continuous) at T_C = 25°C	0.35	0.20	A
I_{DM} (●)	Drain Current (pulsed)	1.4	1	A
P_{TOT}	Total Dissipation at T_C = 25°C	1	0.35	W

(●) Pulse width limited by safe operating area

Table 4: Thermal Data

		TO-92	SOT23-3L	
Rthj-amb	Thermal Resistance Junction-ambient Max	125	357.1 (*)	°C/W
T_J	Operating Junction Temperature	- 55 to 150		°C
T_{stg}	Storage Temperature			

(#) When mounted on 1inch² FR-4, 2 Oz copper board.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125°C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 18 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2.1	3	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 0.5 A		1.8	5	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A		2	5.3	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 10 V , I_D = 0.5 A		0.6		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		43 20 6		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-Off Delay Time Fall Time	V_{DD} = 30 V, I_D = 0.5 A R_G = 4.7Ω V_{GS} = 4.5 V (see Figure 18)		5 15 7 8		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 5 V (see Figure 21)		1.4 0.8 0.5	2	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				0.35 1.40	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 1 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 1 A, di/dt = 100 A/µs, V_{DD} = 20 V, T_j = 150°C (see Figure 19)		32 25 1.6		ns nC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area For TO-92

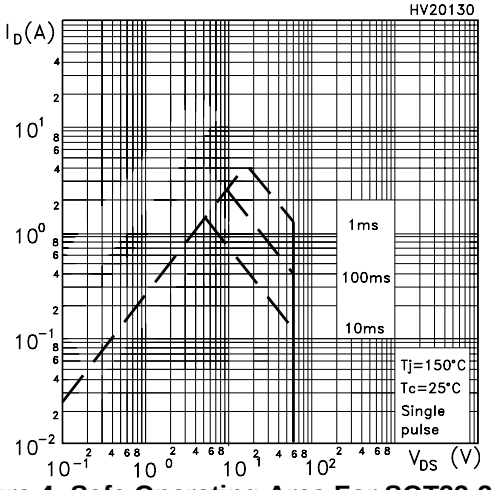


Figure 4: Safe Operating Area For SOT23-3L

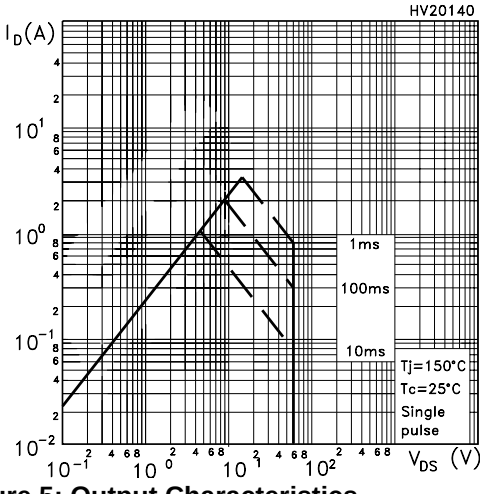


Figure 5: Output Characteristics

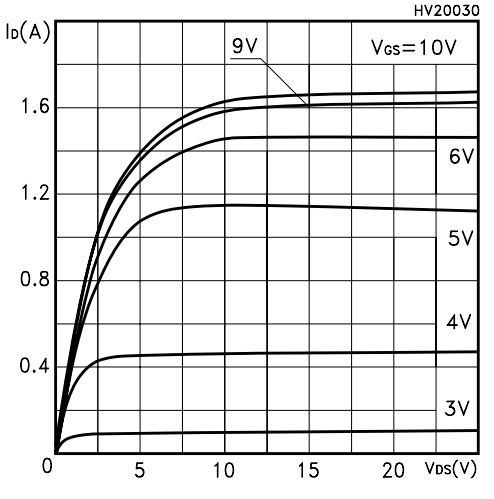


Figure 6: Thermal Impedance For TO-92

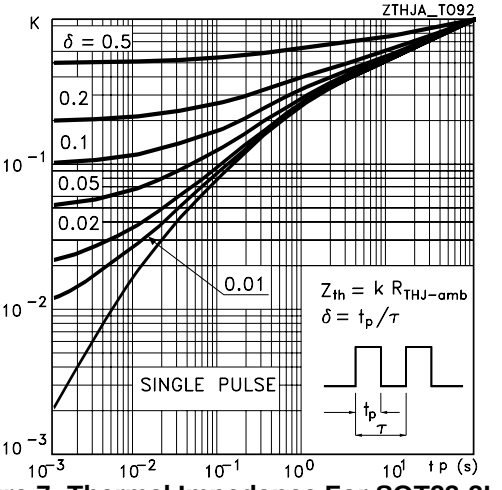


Figure 7: Thermal Impedance For SOT23-3L

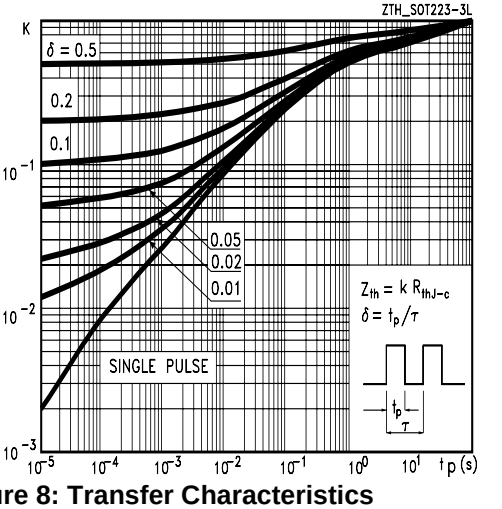


Figure 8: Transfer Characteristics

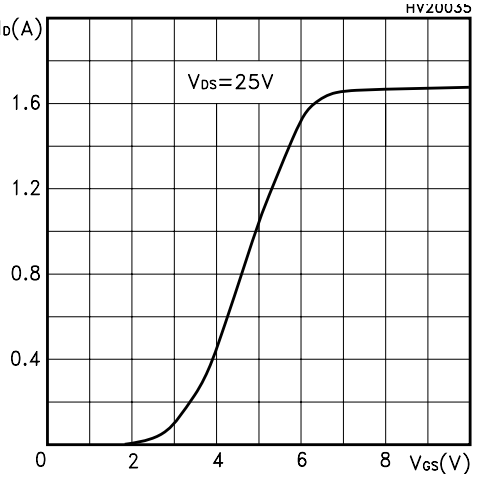


Figure 9: Transconductance

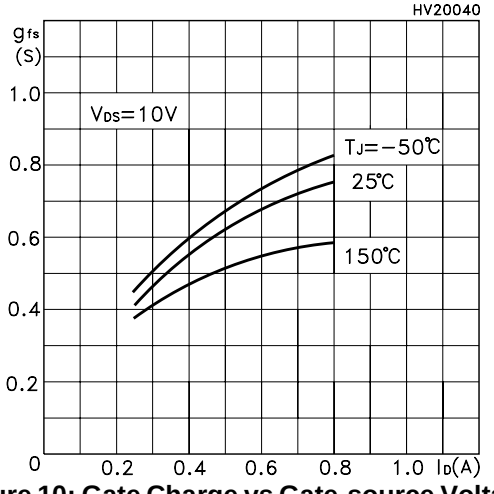


Figure 10: Gate Charge vs Gate-source Voltage

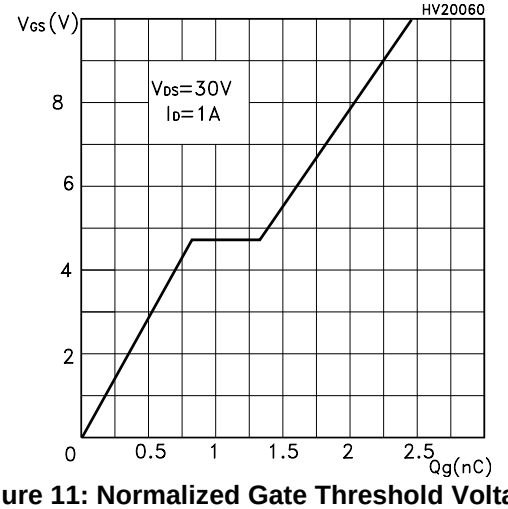


Figure 11: Normalized Gate Threshold Voltage vs Temperature

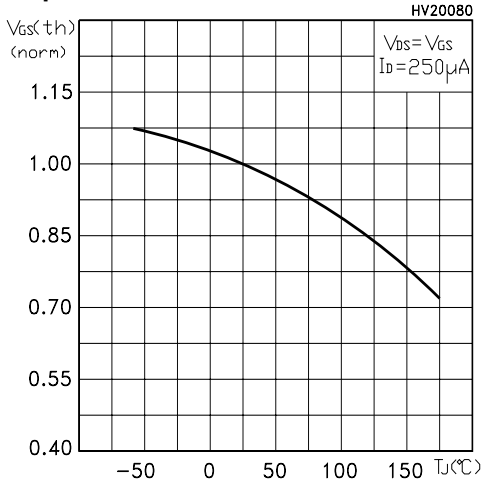


Figure 12: Static Drain-source On Resistance

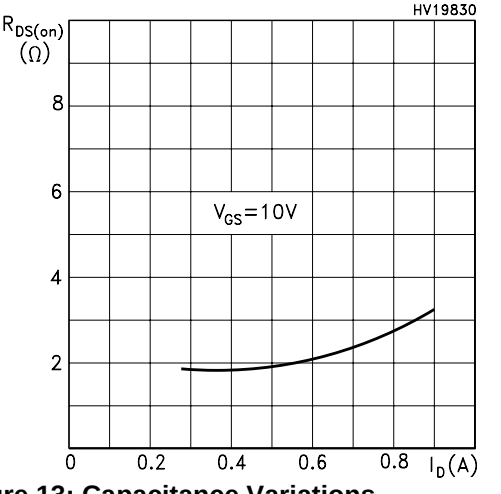


Figure 13: Capacitance Variations

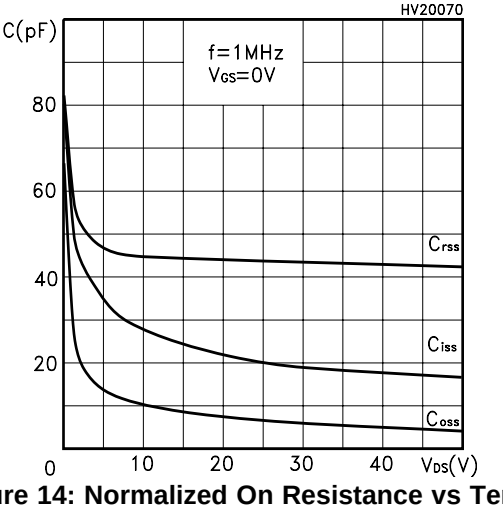


Figure 14: Normalized On Resistance vs Temperature

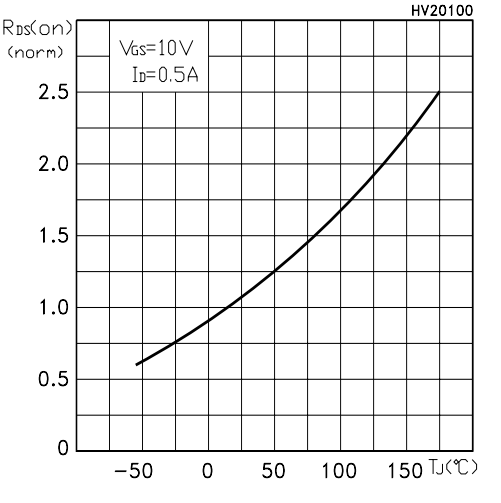


Figure 15: Source-Drain Forward Characteristics

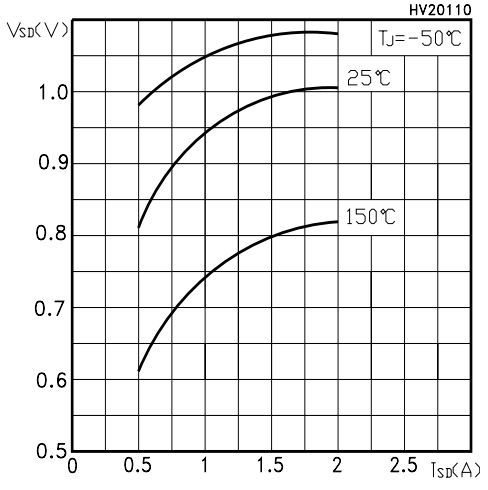


Figure 16: Normalized BVDSS vs Temperature

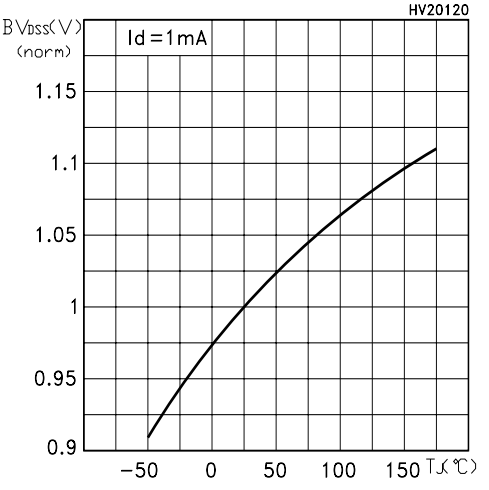


Figure 17: Unclamped Inductive Load Test Circuit

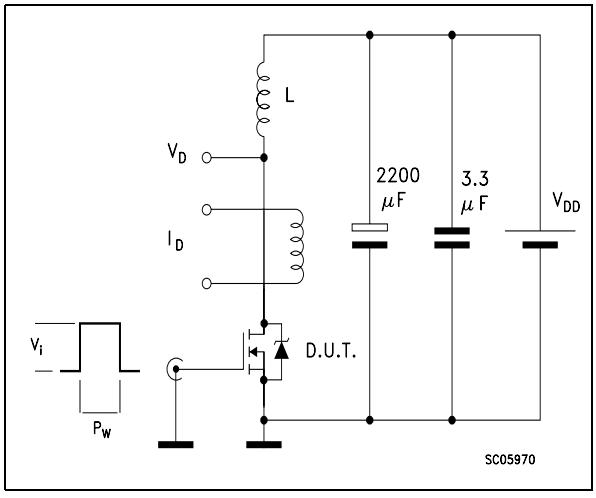


Figure 18: Switching Times Test Circuit For Resistive Load

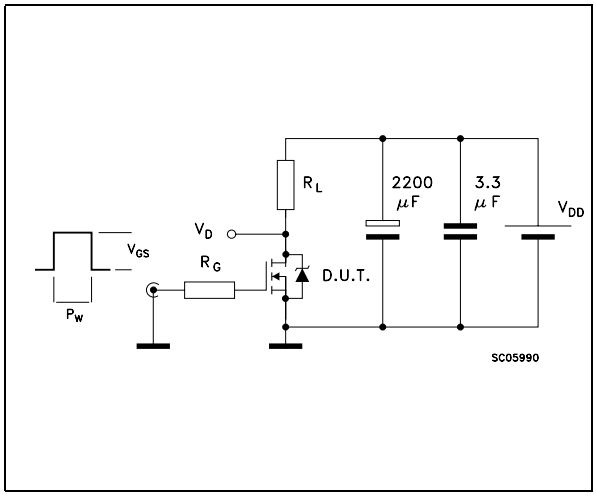


Figure 19: Test Circuit For Inductive Load Switching and Diode Recovery Times

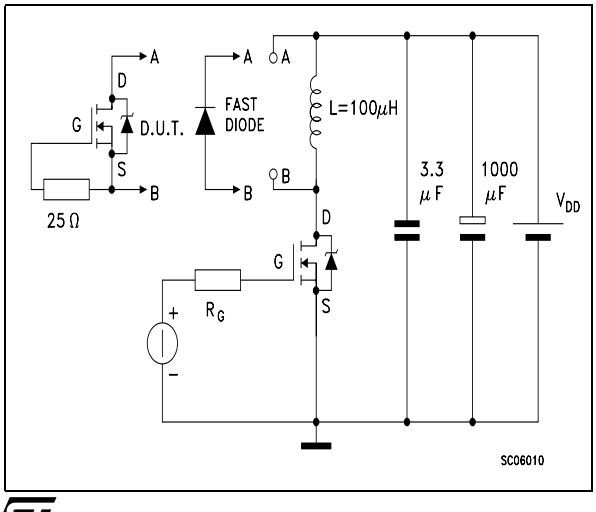


Figure 20: Unclamped Inductive Wafeform

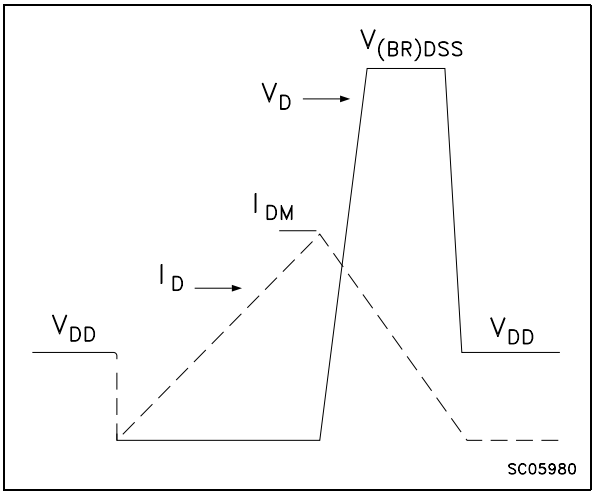
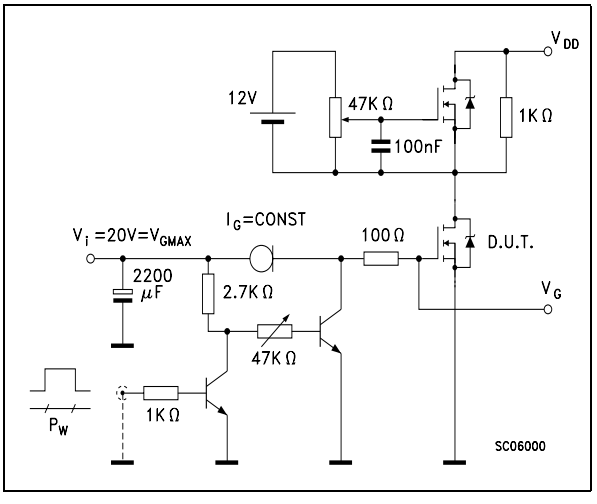
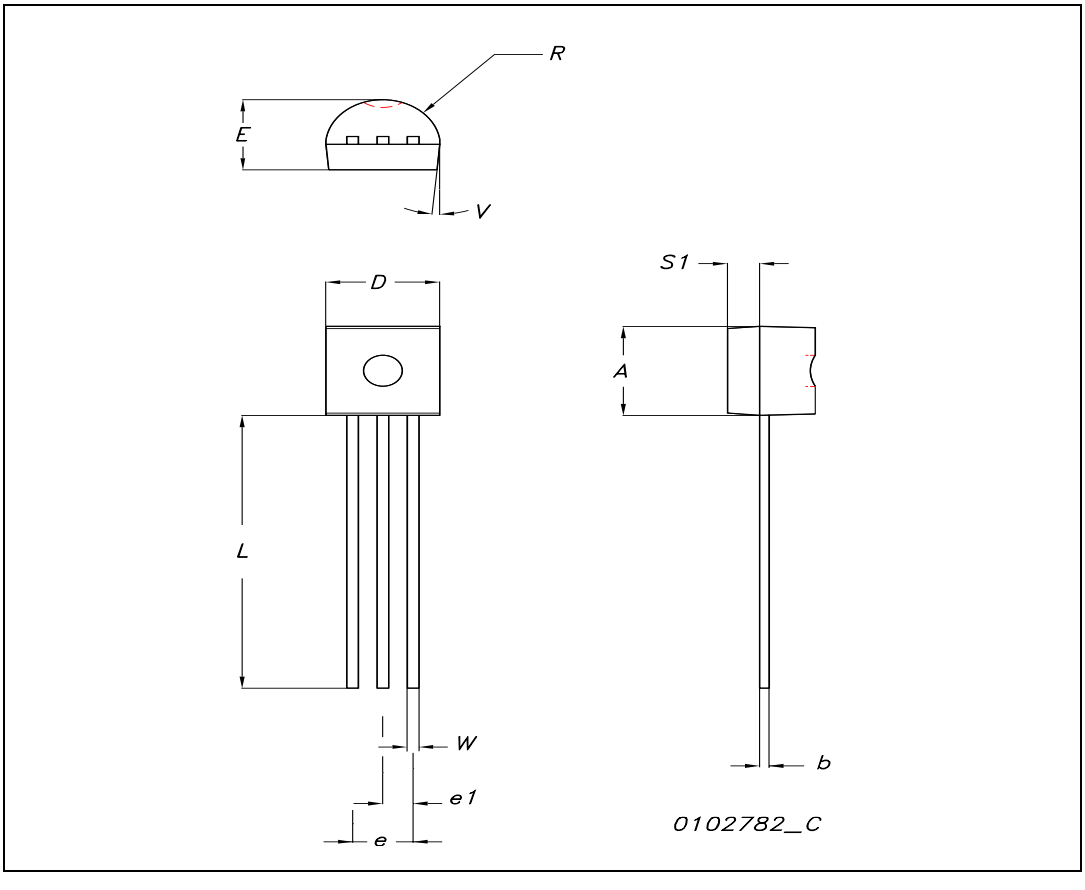


Figure 21: Gate Charge Test Circuit



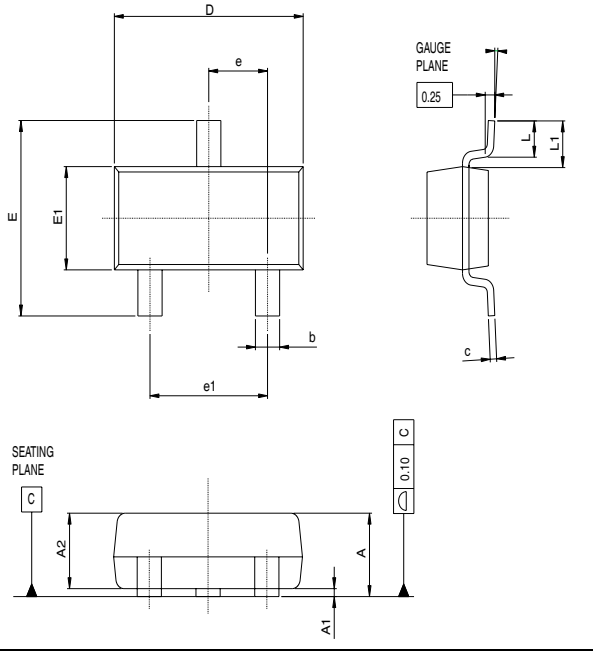
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



SOT23-3L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.890		1.120	35.05		44.12
A1	0.010		0.100	0.39		3.94
A2	0.880	0.950	1.020	34.65	37.41	40.17
b	0.300		0.500	11.81		19.69
C	0.080		0.200	3.15		7.88
D	2.800	2.900	3.040	110.26	114.17	119.72
E	2.100		2.64	82.70		103.96
E1	1.200	1.300	1.400	47.26	51.19	55.13
e		0.950			37.41	
e1		1.900			74.82	
L	0.400		0.600	15.75		23.63
L1		0.540			21.27	
k			8°			8°



7110469/A

Table 8: Revision History

Date	Revision	Description of Changes
06-Apr-2005	2	New stylesheet
20-Apr-2005	3	New Pin Configuration for TO-92

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